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Process Integration of Embedded FeRAMs

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Abstract. This paper describes the general aspects of embedding Ferroelectric Memories (FeRAMs) with logic circuits and/or microcontrollers. These devices and stand-alone memories constitute the main thrust of applications of ferroelectric memories. The problems associated with embedding test the robustness and compatibility of the FeRAM process with established CMOS integrated circuits. As integrated circuits technology advances in lithography, FeRAMs meet the challenge, but new problems appear. In this review, existing embedded FeRAMs of the 0.8/0.6 μ generation will be discussed. A program for the 0.35/0.25 μ generation, and the 0.18 μ challenges are outlined and addressed. The paper also reviews the application of FeRAM Smart Cards. This application is becoming the best example of embedded FeRAMs in which to demonstrate the ''System-One-Chip'' technology direction. Smart Card ICs clearly take advantage of the low power, high-write speed and long endurance characteristics of Ferroelectric Memories.

Keywords: ferroelectric memories, integrated ferroelectrics, embedded microcontrollers, ferroelectric material and integration

1. Introduction

In the last decade, FeRAMs have been demonstrated in ''stand-alone'' and embedded applications. Two materials systems, the perovskites (ABO_3) and the layered perovskites ($A_{(m-1)}\ Bi_2\ B_mO_{(3m+3)}$) constitute two very distinct technologies with different process conditions and capacitor characteristics. This paper discusses only the embedded layered perovskite FeRAMs for reasons that will become clear in section 2 below.

Before we embark on the technological details of the next sections, it is necessary to explain where FeRAMs are today. Since 1993, high-density memory cells using BST ($Ba_{0.7}Sr_{0.3}TiO_3$) demonstrated that ferroelectric materials (although BST is in a para-electric phase) could be integrated in deep submicron schemes (0.14 μ) suitable for gigabit ''stand-alone'' DRAM memories [1]. Thus, at least mechanically, introduction of a capacitor with an ultra-thin (250 Å) complex oxide and the $8F^2$ (where F is the feature length) ''stack cell'' was demonstrated for a volatile memory device. For the non-volatile FeRAM, things are much more difficult. The FeRAM application requires the ferroelectric capacitor to switch and saturate under fields of the order of 200 KV/cm (typically an overdrive of 3–4 times the coercivity) with at least 10^{10} endurance cycles, and no less than 10 years of non-volatile storage at a temperature of at least 70°C. To achieve this with operating voltages below 3 V is the initial challenge of materials and deposition technologies. Our own work in the layered perovskites, as discussed below, demonstrates that this is now possible at full process temperatures around 700°C.

Multi-level metallization is absolutely necessary to achieve embedding of FeRAMs with microcontrollers. Recently [2], a double-level metal FeRAM was demonstrated using layered perovskites. This device was developed for embedding with 8-bit microcontrollers. Mass-production of this device in the 0.8/0.6 μ photolithography generation has already started.

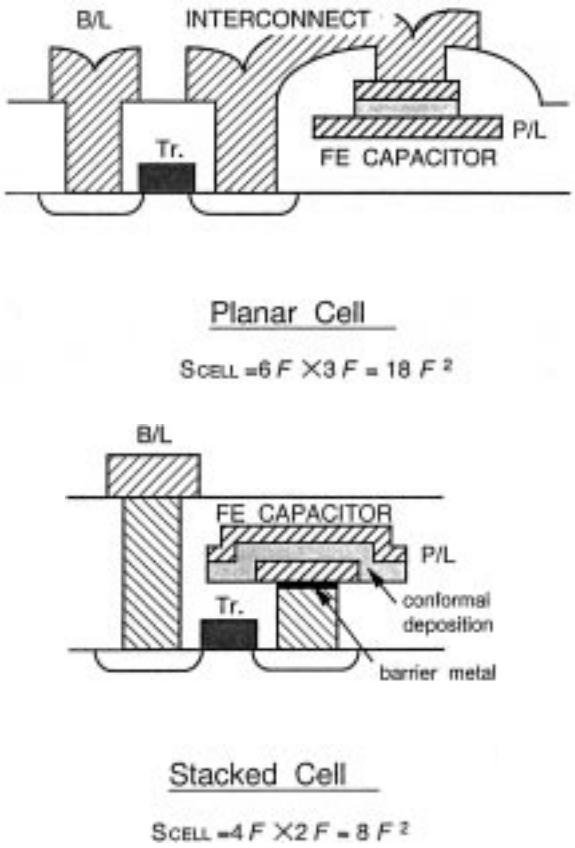

Fig. 1. 1a–strapped cell 1b–stacked cell.

This device uses the common ''strapped cell'' (or capacitor on field oxide) cell architecture. It is therefore safe to say in 1998 that 0.8/0.6 μ technology FeRAMs using the strapped cell (see Fig. 1a) is in mass-production using layered perovskites. It is also fair to say that stand-alone PZT-based devices, using the strapped cell, have been available by Ramtron Corporation in 4–64 Kbits for some time. And, recently, both Fujitsu [3] and NEC [4] have shown 16 Kbit embedded microcontrollers. Of course, these devices are still not in mass-production and appeared two years after the first FeRAM embedded microcontroller was presented by Matsushita in 1996 [5].

In all these schemes, the strapped cell has been used, and lithography in the CMOS side is more aggressive (0.5 μ in the case of [3]) than the ''ferroelectric finishing'' process (which is typically 0.8 μ). The typical cell has been a 2T/2C (two transistors/two capacitors) cell, although 1T/1C experimentation up to 1 Mbits stand-alone have been shown since 1996 for layered perovskites [6] and PZT this year [7]. The key technological milestone of these devices is the ferroelectric thin-film thickness—typically 1800 Å (for layered perovskites) and 2700–3000 Å for PZT for the strapped cell. Thickness in the range of 800–500 Å are needed for the stacked cell, because the capacitor area is so small (in the order of 0.6–0.2 μ^2), that mechanical strength of the high aspect ratio capacitor is a serious issue.

In summary, FeRAMs have to scale in thickness and area in order to become a mainline technology and useful for both stand-alone and embedded applications. This paper shows our scaling data, available deposition processes, cell architecture and device physics issues for the 0.35/0.25 μ and 0.18 μ generations. These line widths correspond with stand-alone memories of the 16 Mbits and 64 Mbits (or larger) generations. It is expected that these devices may appear between the years 2001–02. For embedded applications such as Smart Cards with embedded microcontrollers, the 0.25 μ generation using 32-bit microcontrollers and having 1 Mb FeRAM with 2–3 levels of metallization should become state-of-the-art by early 2000. Until then, by early 1999, commercialization of 8/16-bits CPU with 16/64-kilobit FeRAMs in contactless and contact-type Smart Cards are expected for layered perovskites operating at 3 V or below (without charge pumps). Such devices can start at 0.6 μ process but need to quickly shrink in area in order to meet cost constraints—therefore, the development of 0.35/0.25 μ is now imperative even for low-end applications.

2. Scaling

In the Introduction of this paper, it became clear that BST can scale to 250 Å. And, that 0.35/0.25 μ generations will use the stacked cell. Figure 1b shows a cross-section of such a cell. There are several issues in implementing such a cell using ferroelectric thin-films. They can be summarized as follows

1. The ferroelectric film must deliver the high speed, low voltage, low imprint, long retention, high break-down voltage, low leakage current and better than 10^{12} endurance cycles (with 10^{15} projected with reasonable acceleration factors). This is to be fully verified for thicknesses in the range of 400–800 Å.

Table 1. Status of deposition and ferroelectric thin-film process for submicron FeRAM cells

Deposition techniques	Deposition temperature	Demonstrated line width	Highest annealing temperature	Deposition rate	3 Sigma uniformity	3 Sigma 2 p_r across the wafer	3 Sigma repeat-ability	Electrical data	Through put	Cleaning cycle
LSMCD (PRIMAXX)	RT	Easily cover steps needed for 0.39/0.25 μ generation	700°C (SBT and SBTN)	300–350 Å per minute	1.2%	1.4%	3.5%	Very good down to 450 Å	20–40 wafers per hour	Very clean cold wall process
MOCVD (See Note 1)	400–500°C	0.25 with good step coverage	650–700°C	30–70 Å per minute	N/A (Tool dependent)	N/A (Tool dependent)	N/A	Very good — Higher 2 P_r	N/A	Known to have too much carbon residue

Note 1—This MOCVD data is based on published results by Siemens [8] and other sources. Our own MOCVD data is going to be reported elsewhere [9].

2. The annealing process in oxygen should be around 700°C with a bottom electrode barrier that can stand budget and not allow the poly-silicon layer to oxidize and create a parasitic capacitor.
3. The ferroelectric capacitor should survive the forming gas annealing (95% N_2–5% or less H_2) required by the threshold voltage adjustment of the CMOS process.
4. Etching technology capable of the tolerances required by the stacked cell may need further enhancement, as the cell area becomes smaller.
5. Multi-level metal capability in the FeRAM process.

In the light of the five points above the general direction for FeRAM development is positive because in one form or another these integration issues have been addressed since 1993. But, the deposition technology and basic device physics to guarantee that Item (1) is accomplished with high repeatability, yields and reliability is absolutely necessary.

3. State-of-the-art Layered Perovskites

3.1 Equipment

We have positioned our development strategy for 0.35/0.25 μ and 0.18 μ (or less) generations in two areas. One is the deposition technology and subsequent materials integrity down to 400 Å. The second is lower temperature and smaller thermal budget processes (700–650 Å).

Table I summarizes the status of this strategy as of late 1998. The Primaxx LSMCD (liquid source misted chemical deposition) is already a tool in a mass-production line. Figure 2 shows a picture of this equipment. The key point of LSMCD is that it is already available, has reliable chemical sources, it is clean and has a high deposition rate. In a cluster such as the one shown in Fig. 2, the baking and annealing cycles are all under vacuum and it takes 2–4 min per wafer for the deposition step. Annealing is done with RTA. Extension of LSMCD to 0.18 μ has not been proven yet, but it is not impossible. In section (B) below, we show state-of-the-art data for the LSMCD (Primaxx) process.

In the case of MOCVD, many researchers reported results for SBT and SBTN. However, the best data available for real devices (not just materials studies) was reported by Siemens [8]. Currently, it is known that cleaning of the vaporizer is a limiting factor for

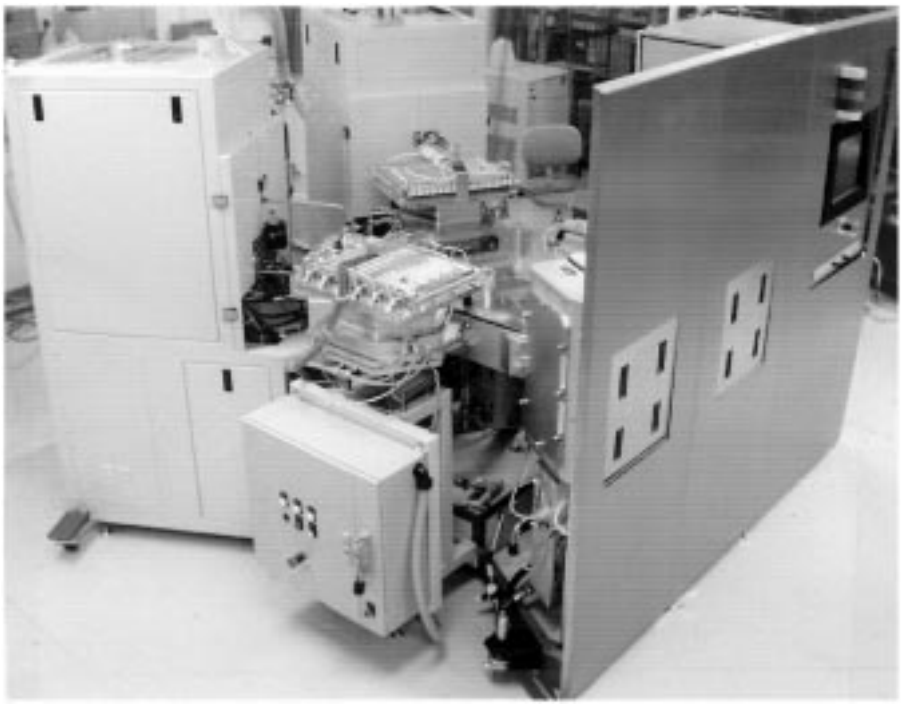

Fig. 2. LSMCD cluster tool by Primaxx.

throughput. Thus, our development program for 1998 focused on the joint design of a new type of MOCVD, which uses a proprietary new delivery system, new short carbon chain sources, a new method of vaporization and an overall new MOCVD chamber built by Aixtron [9].

3.2 LSMCD Data

Figures 3a and 3b show 850 Å data for a typical LSMCD Sr-Bi-Ta-O film with proprietary stoichiometric adjustments. Notice that the film is completely saturated after 1.25 V. A plot of 2 P_r vs. applied voltage is shown in Fig. 4. The highest process temperature of this film is 700°C. Leakage current at 300 KV/cm is 7×10^{-9} Å/cm^2. At 5 volts, the $2P_r$ is 15 μC/cm^2 and the $2E_C$ is 104 KV/cm. These results are shown in Figs. 5a and 5b. Similar results for 475 Å will be published elsewhere [10]. These results are repeatable within 1.4% (3-Sigma).

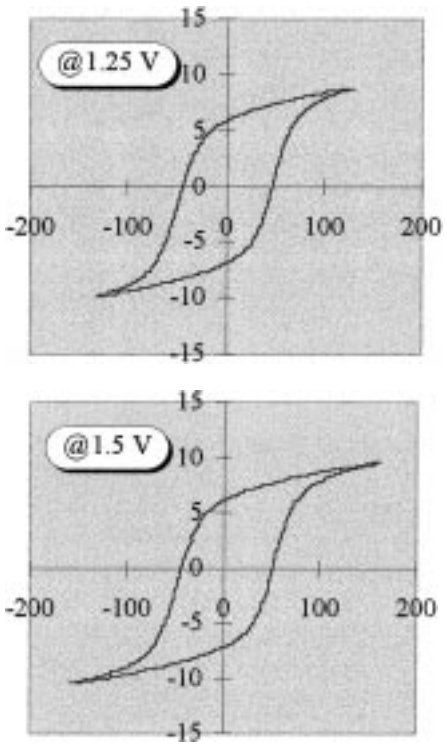

Fig. 3. (a) 1.25 Volts saturated loop of 850 Å SBT film. (b) 1.5 Volts saturated loop of 850 ÅSBT film.

4. Applications

Large-scale manufacturing (over one million devices per month) started at Matsushita Electronics

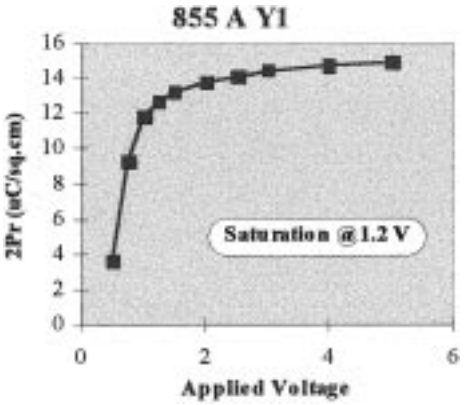

Fig. 4. Voltage scaling for SBT/850 Å/700°C process.

Corporation in July 1998. The first devices were two Smart Cards for non-CPU-required applications. Specification of one of these cards co-designed with Celis Corporation is shown in Fig. 6. Figure 7 shows a layout of this device. Typical use of such a card is ''loyalty programs'', or point cards. With small dye sizes (below 4 mm^2 for 0.8 μ line widths) this device is completely cost competitive with EEPROM-based cards. It is also worth mentioning that due to the fast-write nature of FeRAM, test costs are much lower than for EPPROMs. Thus, with high endurance and 3 V operation this wireless card is very suitable for a variety of applications such as transportation.

A typical, early embedded microcontroller is shown in Fig. 8. Such attempts circa 1996–97 showed the feasibility of embedding SBT/SBTN into a CMOS microcontroller [11]. Following studies in marketing, a Smart Card with CPU was developed at Matsushita. Figure 9 shows an advanced Type B Smart Card aimed at transportation and secure financial transactions. It is interesting to notice that the FeRAM is used as data memory, as well as system configuration memory. A data encryption co-processor is also included using DES schemes. Secured ROM and scratchpad SRAMs are also included, making this device a ''System-on-chip'' demonstration for FeRAMs.

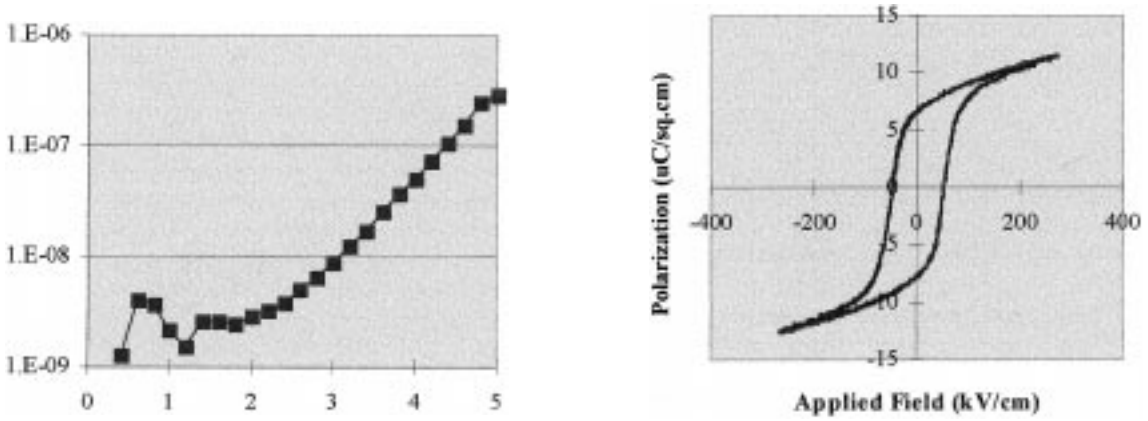

Fig. 5. (a) Leakage current and 3 Volt loops for devices of Figs. 3 and 4. (b) Before and after 10^{10} cycles fatigue test.

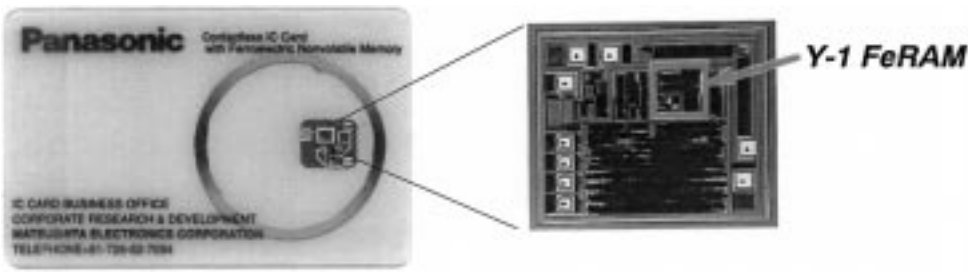

Fig. 6. Matsushita's 1 Kbit card.

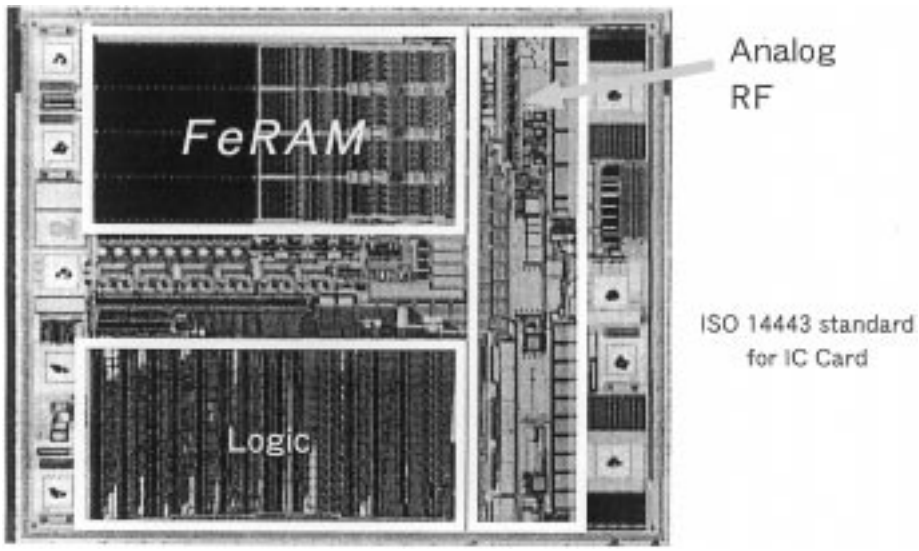

Fig. 7. Layout of 1 Kbit card.

Further embedding with higher FeRAM densities (256 K–1 Mb) for very advanced Smart Cards will take advantage of 0.25 μ line widths and clever cell design. Figure 10 shows a layout of a 1T/1C hybrid cell (''quasi-stacked''), designed by Celis/Hyundai and announced this year in conjunction with Symetrix. This type of device—when implemented in 0.25 μ—is very suitable for embedded microcontrollers. LSMCD implementations of this device showed results comparable with the data described above.

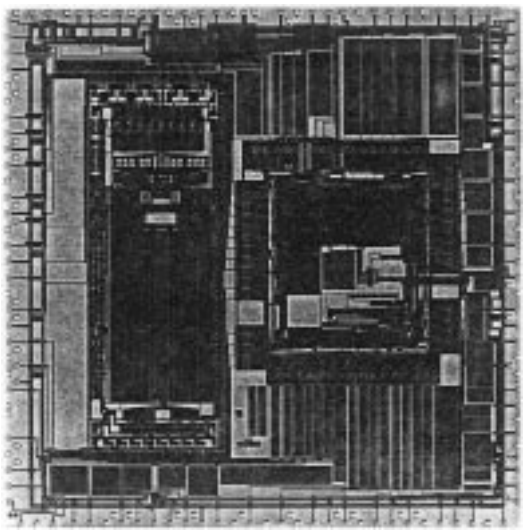

Fig. 8. Early (1997) embedded microcontroller with 4 Kbit FeRAM.

5. Conclusion

This paper describes embedded FeRAMs using state-of-the-art deposition techniques. It also describes the direction of future $8F^2$ cells and current applications. Certain critical areas, such as etching of SBT/SBTN, were not discussed—as were neither detailed proprietary process modules for FeRAM insertion (including annealing schedules) into a CMOS process. Many of these technical issues, such as etching, have been discussed elsewhere [12].

It is clear from the discussion in section 4 that real-world applications, such as Smart Cards and System-on-chip, are entering the market, showing the maturity of FeRAM processes using layered perovskites.

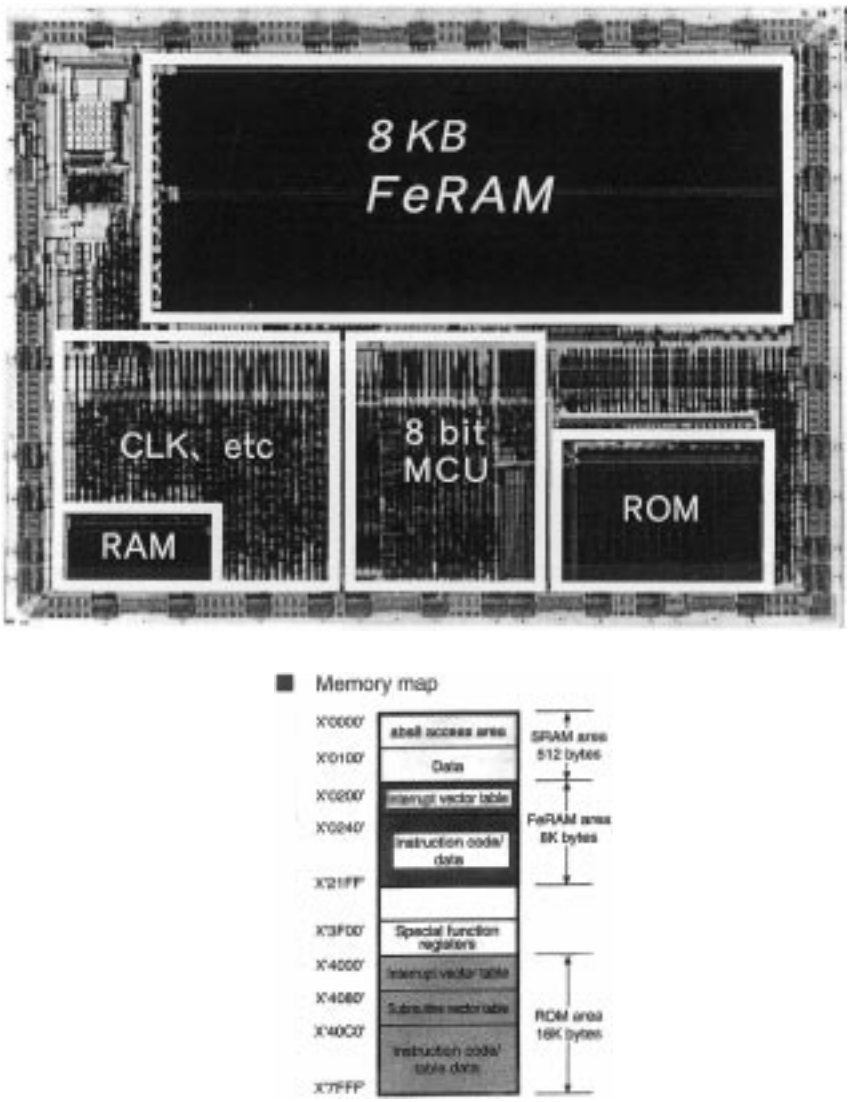

Fig. 9. Advanced Smart Card with 8-bit CPU.

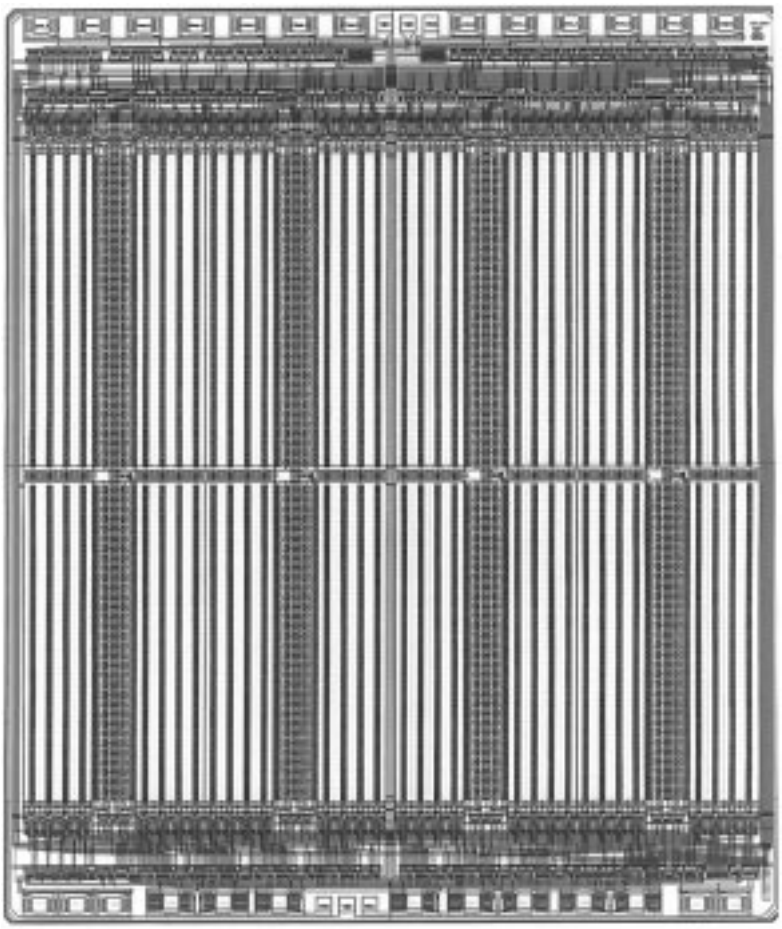

Fig. 10. 256 Kbit FeRAM with ''quasi-stacked cell'' using 1T/1C.

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